Memo

TO: Micah Taylor, Project Lead

FROM: Jeffery Humphrey, Benjamin Efron, Josh Gayso, Thomas Bonatti, Designers

DATE: January 22, 2015

SUBJECT: Milestone II – Register Transfer Language Specification

We have decided to construct our processor as multi-cycle processor. We agreed that it would give us more versatility than a single-cycle processor, and would not be as difficult to implement as a pipeline processor. We agreed upon our eight registers, a couple of which may be swapped out depending on necessity. For all write commands, since everything will be written to our $m register, there will not be a need for a write address. The components of our data path have been tentatively set, including the addition of an adder for branches so we can add PC + immediate without taking up an extra clock cycle. At this point, we only have one pseudo instruction. The addition of pseudo instructions will begin at a later time, the amount is unknown, however, and will depend on how complex the data path ends up being. Our RTL came out fairly straightforward, although might require some slight modification in the future.